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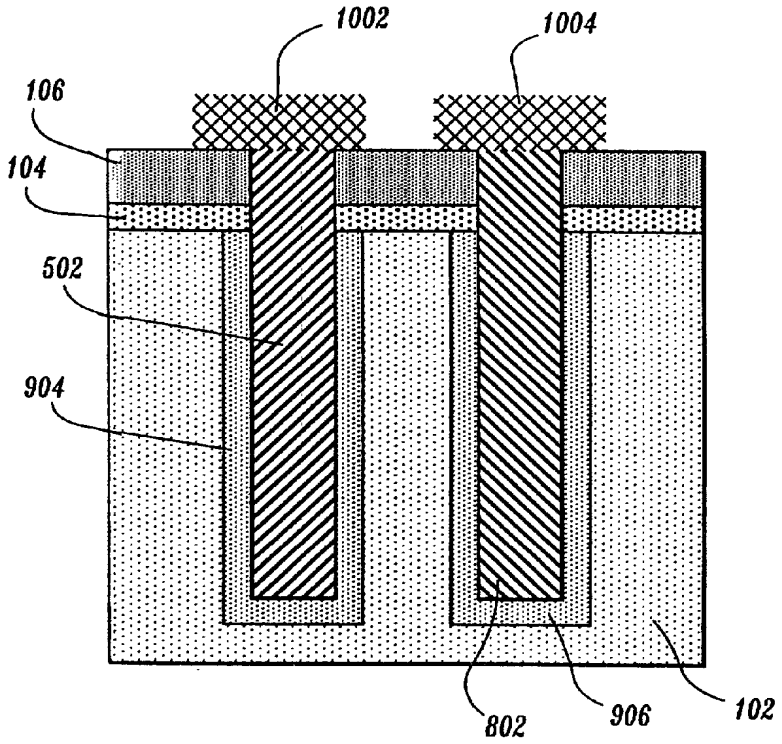
(54) Title: METHODS FOR FORMING LATERAL TRENCH OPTICAL DETECTORS



(57) Abstract: A method for forming an optical detector device on a semiconductor substrate (102). The method includes forming a first set and a second set of trenches in the substrate (102), wherein trenches of the first set are alternately disposed with respect to trenches of the second set, filling the trenches with a sacrificial material (202), and etching the sacrificial material (202) from the first set of trenches. The method further includes filling the first set of trenches with a doped material (502) of a first conductivity, etching the sacrificial material (202) from a second set of trenches, filling the second set of trenches with a doped material (802) of a second conductivity, forming a first junction layer (904) by driving dopants from the doped material (502) in each of the first set of trenches and forming a second junction layer (906) by driving dopants from the doped material (802) in each of the second set of trenches, and providing separate wiring connections (1002, 1004) to the first set of trenches and the second set of trenches. The first and second set of trenches are formed simultaneously.

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METHODS FOR FORMING LATERAL TRENCH OPTICAL DETECTORS

The present invention generally relates to optical detectors, and more particularly, to lateral trench optical detectors formed on a semiconductor opto-electronic integrated circuit.

According to prior art methods of forming trench based optical detectors, in order to form the detector, trenches for different types of electrodes needed to be etched separately, increasing the number of steps in the fabrication process. Because these steps are among the more expensive steps in the fabrication of optical detectors, the production costs reflect the added expense.

Therefore, a need exists for a method of forming a lateral trench p-*i*-n photo-diodes (LTD) wherein the trenches are patterned and then etched for all electrode types simultaneously, i.e. in the same operational step.

According to a first aspect of the present invention a method, of forming an optical detector device on a semiconductor substrate, comprises the steps of:

forming simultaneously a first set and a second set of trenches in the substrate, wherein trenches of the first set are alternately disposed with respect to trenches of the second set;

filling the trenches with a sacrificial material;

etching the sacrificial material from the first set of trenches;

forming a first junction layer, by driving dopants from a first dopant material in each of the first set of trenches and forming a second junction layer, by driving dopants from a second dopant material in each of the second set of trenches; and

providing separate wiring connections to the first set of trenches and the second set of trenches.

According to a second aspect of the present invention, a method, for forming an optical detector device on a semiconductor substrate, comprises the steps of:

forming a first set and a second set of trenches in the substrate, wherein trenches of the first set are alternately disposed with respect to trenches of the second set;

filling the trenches with a sacrificial material;

etching the sacrificial material from the first set of trenches;

filling the first set of trenches with a doped material of a first conductivity;

etching the sacrificial material from a second set of trenches;

filling the second set of trenches with a doped material of a second conductivity;

forming a first junction layer by driving dopants from the doped material in each of the first set of trenches and forming a second junction layer by driving dopants from the doped material in each of the second set of trenches; and

providing separate wiring connections to the first set of trenches and the second set of trenches.

The method includes forming a first set and a second set of trenches in the substrate, wherein trenches of the first set are alternately disposed with respect to trenches of the second set, filling the trenches with a sacrificial material, and etching the sacrificial material from the first set of trenches. The method further includes filling the first set of trenches with a doped material of a first conductivity, etching the sacrificial material from a second set of trenches, filling the second set of trenches with a doped material of a second conductivity, forming a first junction layer by driving dopants from the doped material in each of the first set of trenches and forming a second junction layer by driving dopants from the doped material in each of the second set of trenches, and providing separate wiring connections to the first set of trenches and the second set of trenches.

Preferably, the first set and the second set of trenches in the substrate are formed simultaneously.

Preferably in this second aspect, etching the sacrificial material from the first set of trenches further comprises the steps of removing sacrificial material from a surface of the device, and masking the second set of trenches. Preferably, also, etching the sacrificial material from a second set of trenches includes exposing the sacrificial material of the second set of trenches to a surface of the device.

Providing separate wiring connections may include exposing the doped material filling the first set of trenches and the doped material filling the second set of trenches to a surface of the device, and providing each of the first set of trenches with a first set of contacts and the second set of trenches with a second set of contacts.

Also, in the second aspect, forming the junction layers further may comprise the steps of depositing a diffusion barrier layer over a surface of the device prior to forming the junction layers, and removing the diffusion barrier layer from a surface of the device after forming the junction layers.

Exposing the sacrificial material of the second set of trenches may further include the step of removing the doped material of the first conductivity from a region above the second set of trenches by mechanical polish. Exposing the sacrificial material of the second set of trenches can include patterning the doped material of the first conductivity, and etching the doped material of the first conductivity in a region above the second set of trenches.

The material of the first conductivity may comprises n-type doped polysilicon and the material of the second conductivity p-type doped polysilicon. Alternatively, the material of the first conductivity may comprise p-type doped polysilicon and the material of the second conductivity n-type doped polysilicon.

Preferably the substrate includes a semiconductor material, a SiO_2 layer deposited over the semiconductor material, and a SiN layer deposited over the a SiO_2 layer.

According to a third aspect of the present invention a method, of forming an optical detector device on a semiconductor substrate, comprises the steps of:

forming a first set and a second set of trenches in the substrate, wherein trenches of the first set are alternately disposed with respect to trenches of the second set;

filling the trenches with a sacrificial material of a first conductivity;

etching the sacrificial material from the first set of trenches;

filling the first set of trenches with a doped material of a second conductivity;

forming a first junction layer by driving dopants from the doped material in each of the first set of trenches and forming a second junction layer by driving dopants from the sacrificial material in each of the second set of trenches;

etching the sacrificial material from the second set of trenches;

filling the second set of trenches with an electrode material; and

providing separate wiring connections to the first set of trenches and the second set of trenches.

The method includes forming a first set and a second set of trenches in the substrate, wherein trenches of the first set are alternately disposed with respect to trenches of the second set, filling the trenches with a sacrificial material of a first conductivity, and etching the sacrificial material from the first set of trenches. The method further includes filling the first set of trenches with a doped material of a second conductivity, forming a first junction layer by driving dopants from the doped material in each of the first set of trenches and forming a second junction layer by driving dopants from the sacrificial material in each of the second set of trenches, etching the sacrificial material from the second set of trenches, filling the second set of trenches with an electrode material, and providing separate wiring connections to the first set of trenches and the second set of trenches.

Preferably, in this third aspect, etching the sacrificial material from the first set of trenches further includes removing sacrificial material from a surface of the device, and masking the second set of trenches.

Prior to forming the junction layers, the doped material of the second conductivity is preferably removed from a surface of the device. Forming junction layers preferably further includes depositing a diffusion barrier layer over the surface of the device prior to forming the junction layers, and removing the diffusion barrier layer from a surface of the device after forming the junction layers.

Providing separate wiring connections may further comprise the step of exposing the doped material filling the first set of trenches and the electrode material filling the second set of trenches to a surface of the device. The electrode material may be one of doped material of the first conductivity and undoped material.

According to a fourth aspect of present invention, a method, for forming an optical detector device on a semiconductor substrate, comprises the steps of:

forming a first set and a second set of trenches in the substrate, wherein trenches of the first set are alternately disposed with respect to trenches of the second set;

filling the trenches with a sacrificial material;

etching the sacrificial material from the first set of trenches;

forming a junction layer in the wall of each of the first set of trenches by gas phase doping;

forming a second junction layer in each wall of each of the second set of trenches; wherein dopants are driven from the sacrificial material into the walls;

filling the first set of trenches with a doped material of a first conductivity;

etching the sacrificial material from the second set of trenches;

filling the second set of trenches with a doped material of a second conductivity; and

providing separate wiring connections to the first set of trenches and the second set of trenches.

The method includes forming a first set and a second set of trenches in the substrate, wherein trenches of the first set are alternately disposed with respect to trenches of the second set, filling the trenches with a sacrificial material, and etching the sacrificial material from the first set of trenches. The method further includes forming a junction layer in the wall of each of the first set of trenches by gas phase doping, forming a second junction layer in the wall of each of the second set of trenches, wherein dopants are driven from the sacrificial material into the walls, filling the first set of trenches with a doped material of a first conductivity, etching the sacrificial material from the second set of trenches, filling the second set of trenches with a doped material of a second conductivity, and providing separate wiring connections to the first set of trenches and the second set of trenches.

Preferably, etching the sacrificial material from the first set of trenches includes removing the sacrificial material from a surface of the device, and masking the second set of trenches. Etching the sacrificial material from the second set of trenches further comprises the step of removing doped material of the first conductivity from a surface of the device.

Providing separate wiring connections includes exposing the doped material filling the first set of trenches and the doped material filling the second set of trenches to a surface of the device.

For a better understanding of the present invention, by way o example, preferred embodiments of the invention will be described below in more detail, with reference to the accompanying drawings, in which:

Fig. 1 is a cross-sectional view of a lateral trench in a semiconductor substrate;

Fig. 2 is a cross-sectional view of the lateral trench semiconductor substrate of Fig. 1, wherein a plurality of trenches are filled with a sacrificial material;

Fig. 3 is a cross-sectional view of the lateral trench semiconductor substrate of Fig. 2, wherein the exposed sacrificial material is polished;

Fig. 4 is a cross-sectional view of the lateral trench semiconductor substrate of Fig. 3, wherein the sacrificial material is removed from a first set of trenches;

Fig. 5 is a cross-sectional view of the lateral trench semiconductor substrate of Fig. 4, wherein a n+ poly is deposited over the surface of the device;

Fig. 6 is a cross-sectional view of the lateral trench semiconductor substrate of Fig. 5, wherein the n+ poly is patterned;

Fig. 7 is a cross-sectional view of the lateral trench semiconductor substrate of Fig. 6, wherein the sacrificial material is removed from a second (first) set of trenches;

Fig. 8 is a cross-sectional view of the lateral trench semiconductor substrate of Fig. 7, wherein a p-type poly is deposited over the entire surface of the device;

Fig. 9 is a cross-sectional view of the lateral trench semiconductor substrate of Fig. 8, wherein n and p junction layers have been formed;

Fig. 10 is a cross-sectional view of the lateral trench semiconductor substrate of Fig. 9, wherein metal contacts are patterned over the doped regions;

Fig. 11 is a cross-sectional view of a lateral trench semiconductor substrate in accordance with another embodiment of the present invention, wherein a TEOS diffusion barrier layer is deposited over the device;

Fig. 12 is cross-sectional view of the lateral trench semiconductor substrate of Fig. 11, wherein the TEOS diffusion barrier layer has been removed after drive-in anneal from the first doped electrode material (n+ poly) and the sacrificial material; and

Fig. 13 is a cross-sectional view of a lateral trench semiconductor substrate in accordance with a further embodiment of the present invention, wherein dopants are driven into a second set of trenches by using Gas Phase Doping and into a first set of trenches from sacrificial material.

An optical detector is formed on a semiconductor substrate by forming a plurality of substantially parallel trenches in the substrate to form a plurality of regions separated by alternating trench regions of

n-type and p-type doped material. The n-type regions are connected together to form an n-contact. The p-type regions are connected together to form a p-type contact. The regions separating the trenches function as intrinsic semiconducting layer (*i*), thereby forming a plurality of parallel p-*i*-n photo-diodes. The basic principle behind this detector topology is to move free carriers in the absorption region of the detector in a direction perpendicular to the incident light.

The present invention discloses a method of optical detector formation in which trenches for both n-type and p-type doped material are patterned and then etched at the same time to form a desired interdigitated photo-diode device. The desired structure can then be achieved by plugging a first set of trenches with a sacrificial layer, while filling a second set with an electrode material (e.g., polysilicon). Thus, the present invention proposes a method of forming a lateral trench optical detector wherein a first and a second set of trenches are patterned and then etched simultaneously. By reducing the number of lithographic patterning and deep trench etching steps in the photo-detector fabrication process, the present invention may reduce production costs.

Referring to Fig. 1, according to an embodiment of the present invention, deep trenches are patterned and etched in a semiconductor substrate (102) using, for example, reactive ion etching (RIE). These deep sets of trenches, only one of each set of which is shown in the drawing figures, will form alternating n-type and p-type electrodes of a lateral trench photo-detector device. The substrate can also include a pad layer (104) formed of, for example, SiO_2, and a SiN layer (106) deposited over the SiO_2 for use as a chemical-mechanical-polishing (CMP) stop. One skilled in the art would recognise in light of the present invention that other substrates can be used without departing from the scope and spirit of the present invention, for example, silicon germanium, germanium, and single-crystal silicon.

Referring to Fig. 2, the trenches are then filled with a sacrificial material (202), such as an oxide (borosilicate glass (BSG), phosphosilicate glass (PSG), Arsensilicate glass(ASG), borophosphosilicate glass (BPSG), tetraorthosilicate (TEOS), etc.). Preferably, the oxide has high etch selectivity to the substrate (102). The sacrificial material may be polished (e.g., CMP) to the underlying SiN layer.

Referring to Fig. 3, alternating trenches are masked using, for example, an amorphous Si (302). The mask material (302) is deposited over the surface of the device and then the mask material (302) over the alternating trenches is removed to expose the underlying sacrificial material (202). The sacrificial material (202) is then etched out of the first set of trenches (Fig. 4).

Referring to Fig. 5, the device is covered with a first doped electrode material (502), filling the open trenches. Doped material such as n-type or p-type doped polysilicon can be used. The sacrificial material (202) that was previously masked continues to plug a second set of trenches and keeps the first electrode material (502) from filling the second set of trenches. The electrode material (302) (poly) over the second set of trenches with sacrificial material fillings can then be patterned and etched. Alternatively, the method can include mechanically polishing and planarizing the device to remove the electrode material that overhangs outside the trenches. Either means may be used to cause the sacrificial material filling in the second set of trenches to be exposed to the surface of the device. (Fig. 6) The first set of trenches may then be masked prior to removing the sacrificial material from the second set of trenches. The sacrificial material can be removed by an etch process such as wet etching. (Fig. 7) Thereafter, as shown in Fig. 8, the second set of trenches are filled with a second type of electrode material (802) such as n-type or p-type doped polysilicon. Any excess electrode material outside trenches can be removed by planarization.

Referring to Fig. 9, after planarization, a TEOS diffusion barrier layer (902) is deposited over the device and the dopants are driven into the substrate surrounding the n-type and p-type doped trenches forming the n-type junction (904) and p-type junction (906), respectively. After annealing, the TEOS diffusion barrier layer (902) is removed and metal contacts (1002, 1004) are applied to the electrodes. (Fig. 10)

Referring to Fig. 11, according to an alternative embodiment of the present invention, after filling a first set of trenches with an n-type polysilicon (502) and patterning (as Fig. 6), a TEOS diffusion barrier layer (902) can be deposited over the surface of the device. By using the sacrificial material (202) (e.g., BSG) in a second set of trenches as a p-type dopant source, and a drive-in anneal, an n-type junction (904) and a p-type junction (906) can be formed by out-diffusion from the n-type doped material (502) and the sacrificial material (202), respectively. The TEOS diffusion barrier layer (902) can then be removed. (Fig. 12).

Referring to Fig. 13, according to a further embodiment of the present invention, after etching a sacrificial material from a first set of alternating trenches (as Fig. 4), dopants are driven into the first set of trenches by using Gas Phase Doping forming a first junction type (904). Dopants are driven into a second set of trenches from the sacrificial material (202) forming a second junction type (906). The first set of trenches are filled with a first electrode material, excess electrode material covering the second set of trenches is removed. The sacrificial material (302) covering the second set of trenches is etched and the second set of trenches is filled with a second doped electrode material. The first doped electrode material of the first set of trenches is exposed to the surface of the device and wiring connections (contacts, etc.) are provided.

A lateral trench photo-detector has been fabricated according to the present invention on a p-type silicon substrate with a resistivity of 11 to 16W-cm, wherein trenches were 8μm deep and 0.35μm wide, and further having a spacing of 3.3μm between trenches. The device was a circle with a diameter of 75μm. Borosilicate glass (BSG) was used as the sacrificial material, while a first set of trenches was filled with phosphorous-doped polysilicon ($\sim 10^{20} cm^{-3}$) and a second set of trenches was filled with boron-doped polysilicon ($\sim 10^{18} cm^{-3}$). The device was annealed at 1000^{N}C in Argon for ten minutes to drive the dopant into the substrate and avoid forming junctions at the silicon/polysilicon interface. Silicide and metal contacts were formed on top of each trench electrode.

Some results have shown that the DC I-V characteristics for the lateral trench photo- detector include currents of 1.5pA and 3pA at -5V and -15V respectively. The breakdown voltage was approximately -27V. The series resistance of the lateral trench photo-diode extracted from the forward biased 1-V curve is 15W. The responsivity is 045A/W at 845nm, independent of the bias voltage. The external quantum efficiency was observed to be sixty-six percent. For a device in accordance with the present invention, responsivity is constant over a frequency range from DC to a -3dB bandwidth of 2.8GHZ for a light source at 670nm.

By wiring the discrete photo detector with a 2.5Gb/s BiCMOS preamplifier, at a bit-error- rate of 10^{-9}, a receiver showed a sensitivity of -16.1dBm at 2.5Gb/s and -15.4dBm at 3Gb/s for a bias of 3.3V. With an increase of the bias to -5.0V, the sensitivity may be improved to -16.4dBm at 2.5Gb/s.

Having described embodiments of a method for forming a lateral trench photo-detector, it is noted that modifications and variations can be made by persons skilled in the art in light of the above teachings. It is therefore to be understood that changes may be made in the particular embodiments of the invention disclosed which are within the scope of the invention as defined by the appended claims. claims.

CLAIMS

1. A method of forming an optical detector device on a semiconductor substrate, comprising the steps of:

forming simultaneously a first set and a second set of trenches in the substrate, wherein trenches of the first set are alternately disposed with respect to trenches of the second set;

filling the trenches with a sacrificial material;

etching the sacrificial material from the first set of trenches;

forming a first junction layer, by driving dopants from a first dopant material in each of the first set of trenches and forming a second junction layer, by driving dopants from a second dopant material in each of the second set of trenches; and

providing separate wiring connections to the first set of trenches and the second set of trenches.

2. A method according to claim 1, wherein prior to forming the junction layers, the method includes the further steps of:

filling the first set of trenches with said first dopant material, which is of a first conductivity type;

etching the sacrificial material from the second set of trenches; and

filling the second set of trenches with said second dopant material, which is of a second conductivity type.

3. A method according to claim 1, wherein the sacrificial material comprises said second dopant material and the second junction layer is formed by driving the dopants from the sacrificial layer in the second set of trenches.

4. A method according to claim 3, wherein, prior to forming the junction layers, the method includes the further step of:

filling the first set of trenches with said first dopant material, with the first dopant material being of a first conductivity type and said sacrificial layer being of a second conductivity type.

5. A method according to claim 4, further including the steps of:

following the formation of the junction layer in the second set of trenches, etching the sacrificial layer from the second set of trenches; and

filling the second set of trenches with an electrode material.

6. A method according to claim 3, wherein said first dopant material is a gas dopant and said junction layer is formed in said first set of trenches by gas phase doping and wherein the method includes the further steps of:

filling the first set of trenches with doped material of a first conductivity type;

etching the sacrificial material from the second set of trenches; and

filling the second set of trenches with a doped material of a second conductivity type.

7. A method according to any preceding claim , wherein the step of etching the sacrificial material from the first set of trenches further comprises the steps of:

removing sacrificial material from a surface of the device; and

masking the second set of trenches.

8. A method according to claim 7, wherein the step of etching the sacrificial material from the second set of trenches further comprises the step of exposing the sacrificial material of the second set of trenches to a surface of the device.

9. A method according to any preceding claim, wherein the step of providing separate wiring connections further comprises the steps of:

exposing the material filling the first set of trenches and the material filling the second set of trenches to a surface of the device; and

providing each of the first set of trenches with a first set of contacts and the second set of trenches with a second set of contacts.

10. A method according to claim 2 or 4, wherein the step of forming the junction layers further comprises the steps of:

depositing a diffusion barrier layer over a surface of the device prior to forming the junction layers; and

removing the diffusion barrier layer from a surface of the device after forming the junction layers.

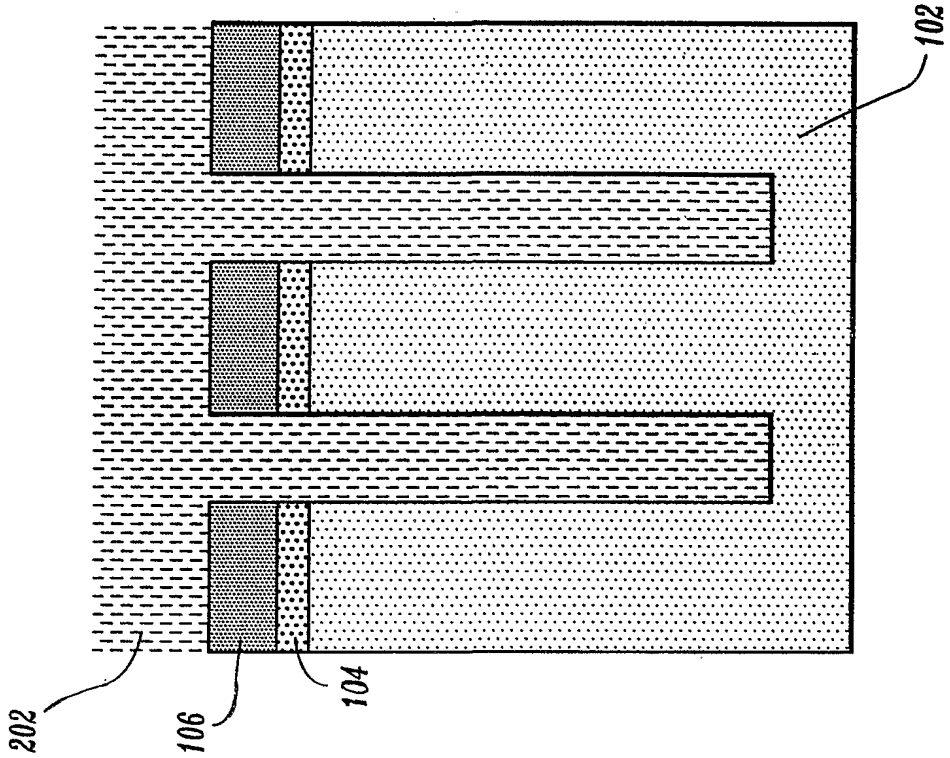


FIG. 2

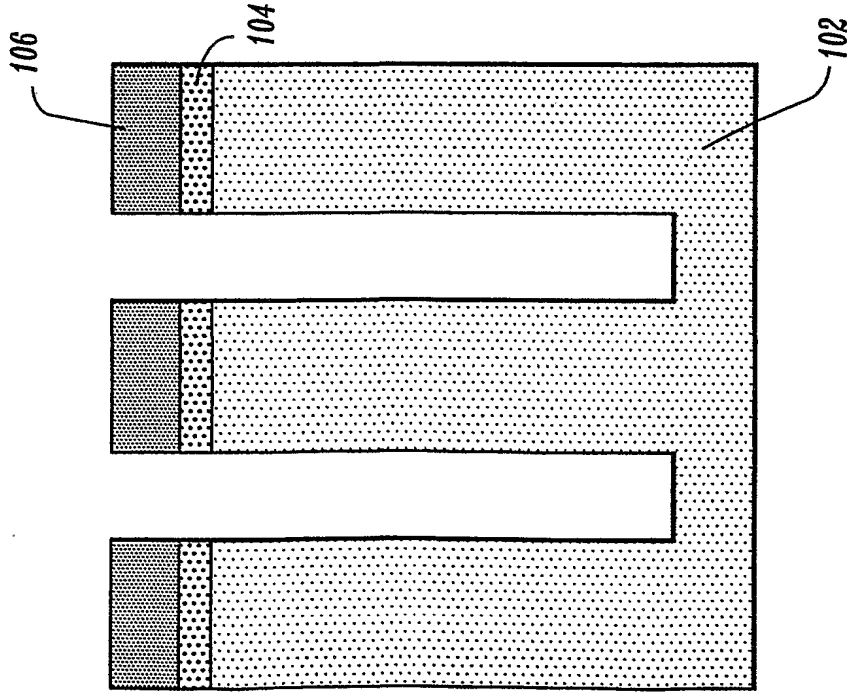


FIG. 1

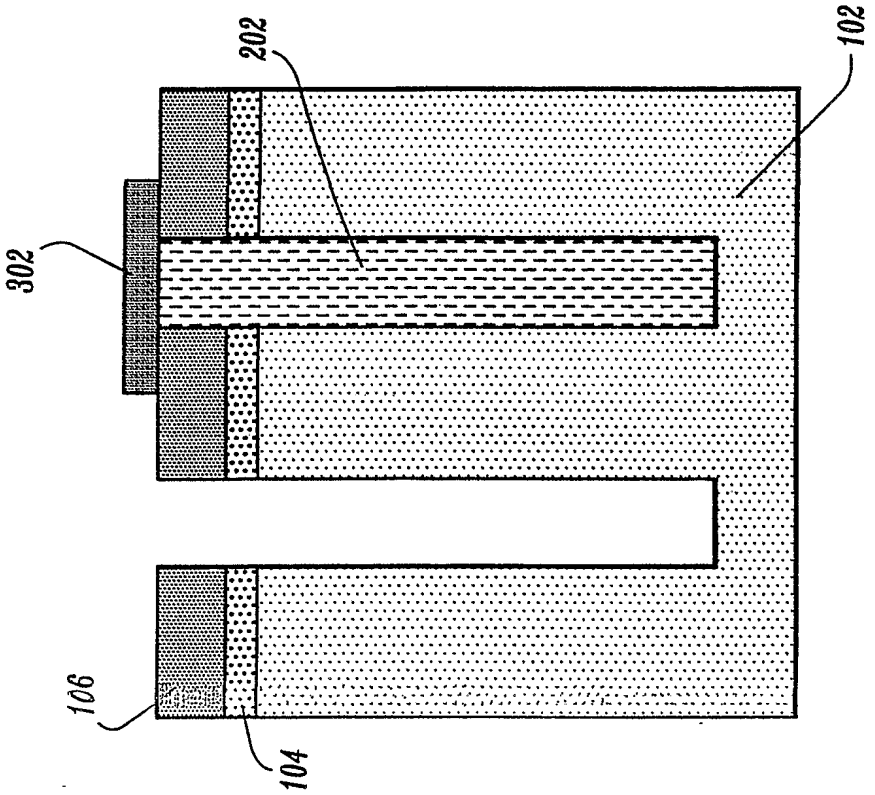


FIG. 4

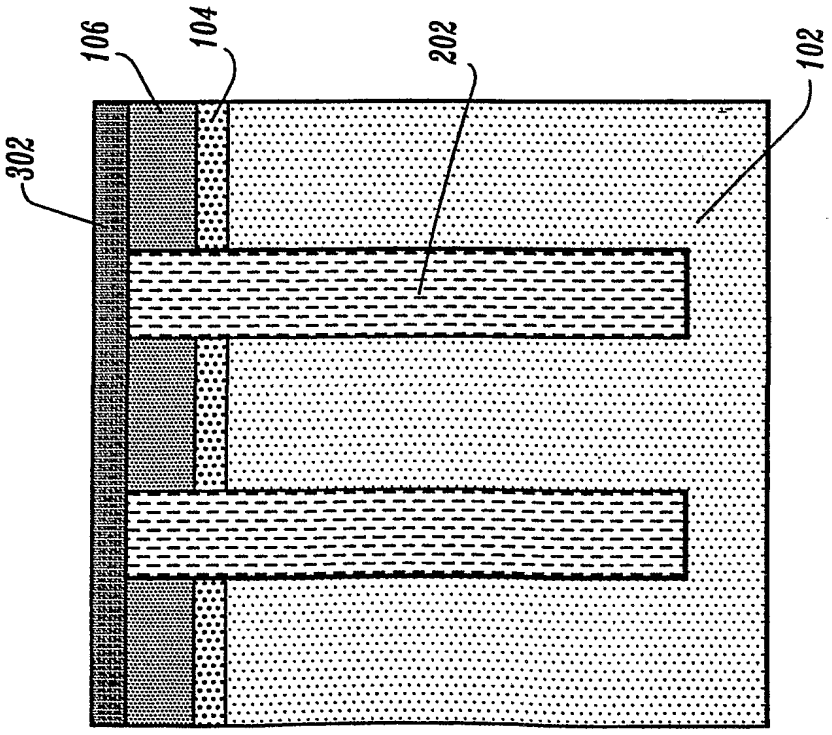


FIG. 3

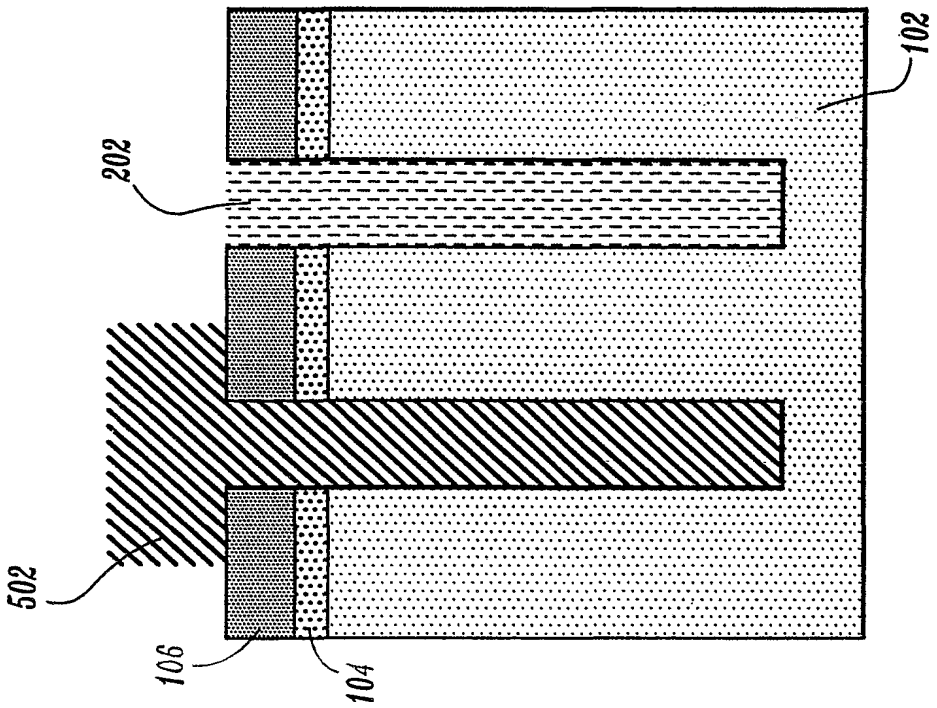


FIG. 6

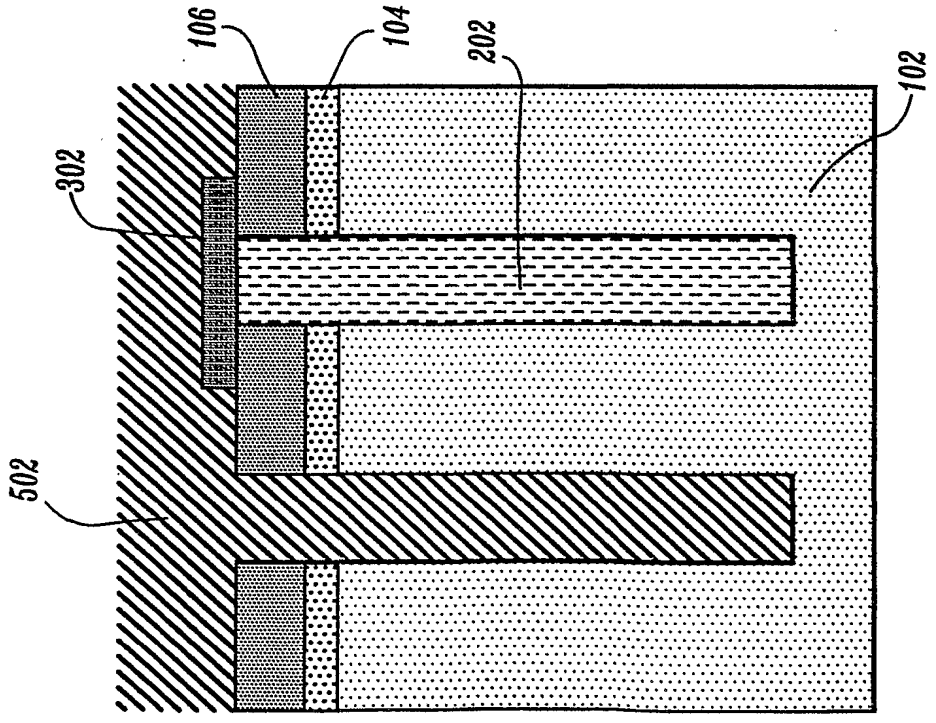


FIG. 5

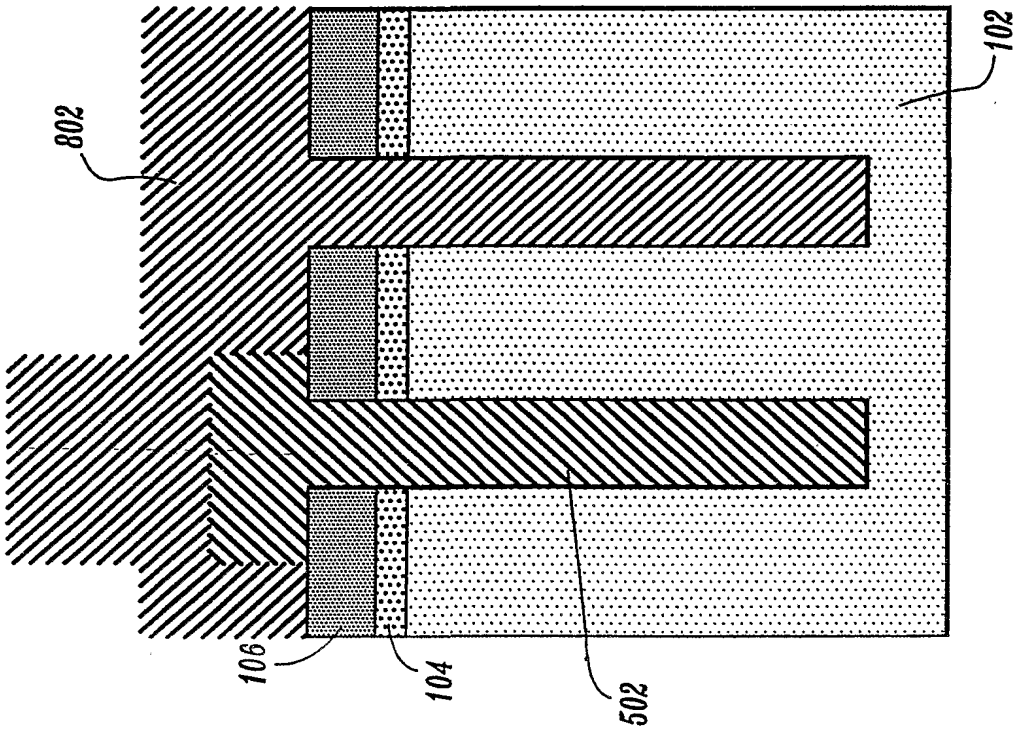


FIG. 8

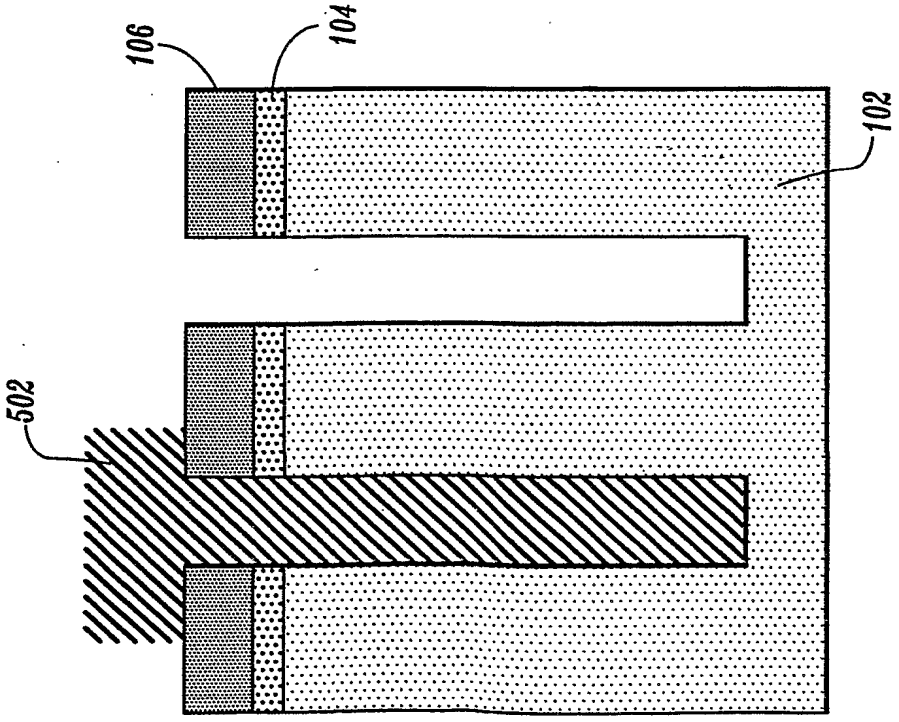


FIG. 7

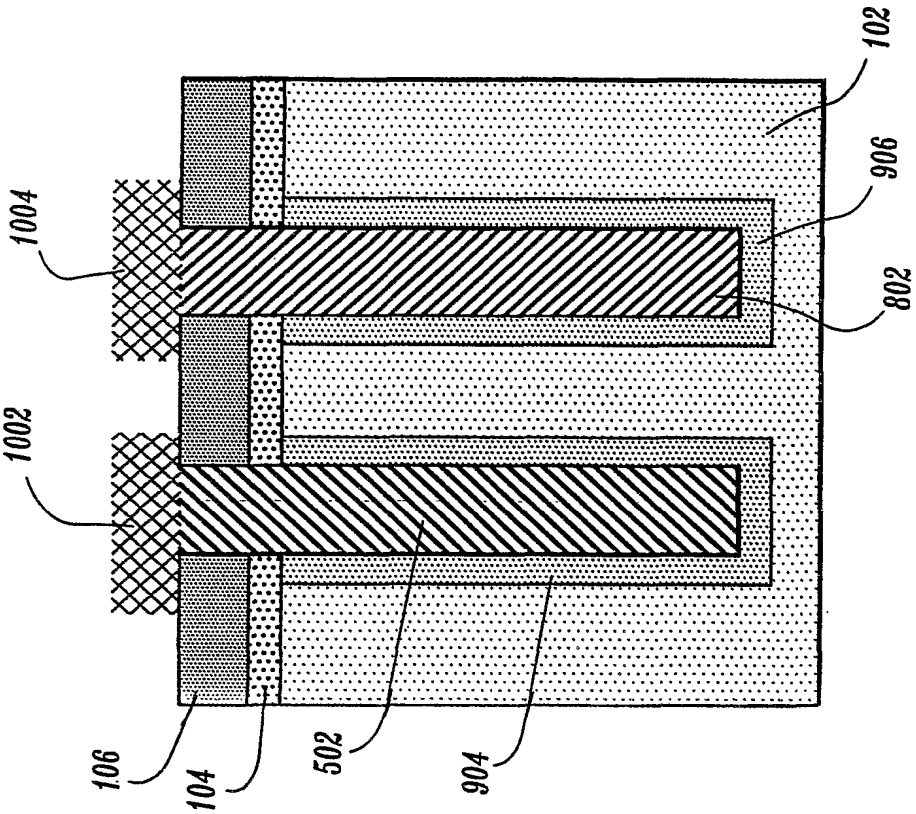
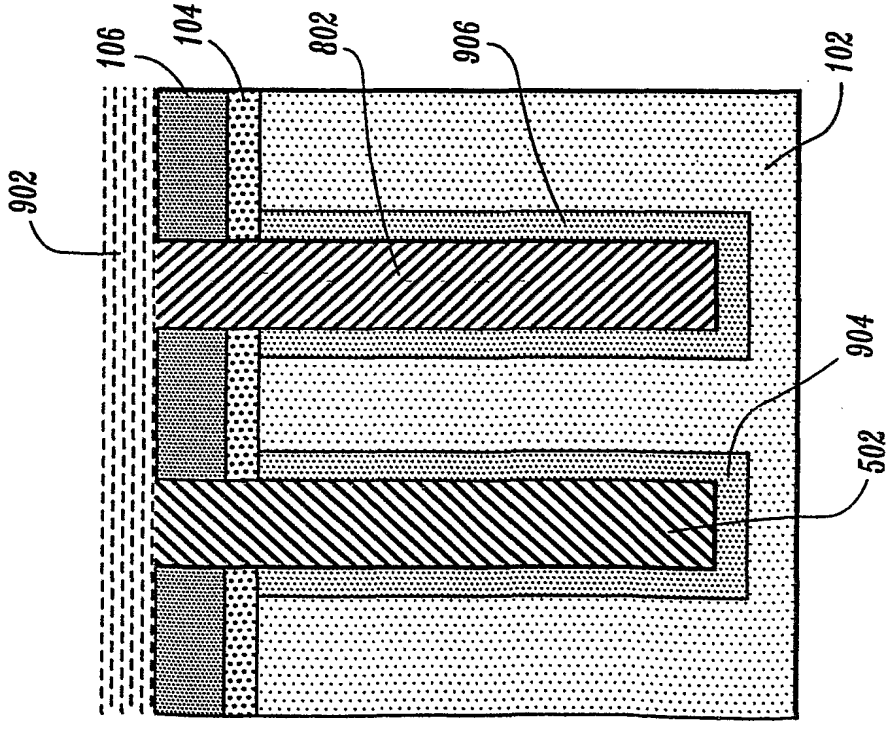

102
906
1004
802
1002
106
104
502
904

FIG. 10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104
802
906
102
902
904
502

FIG. 9

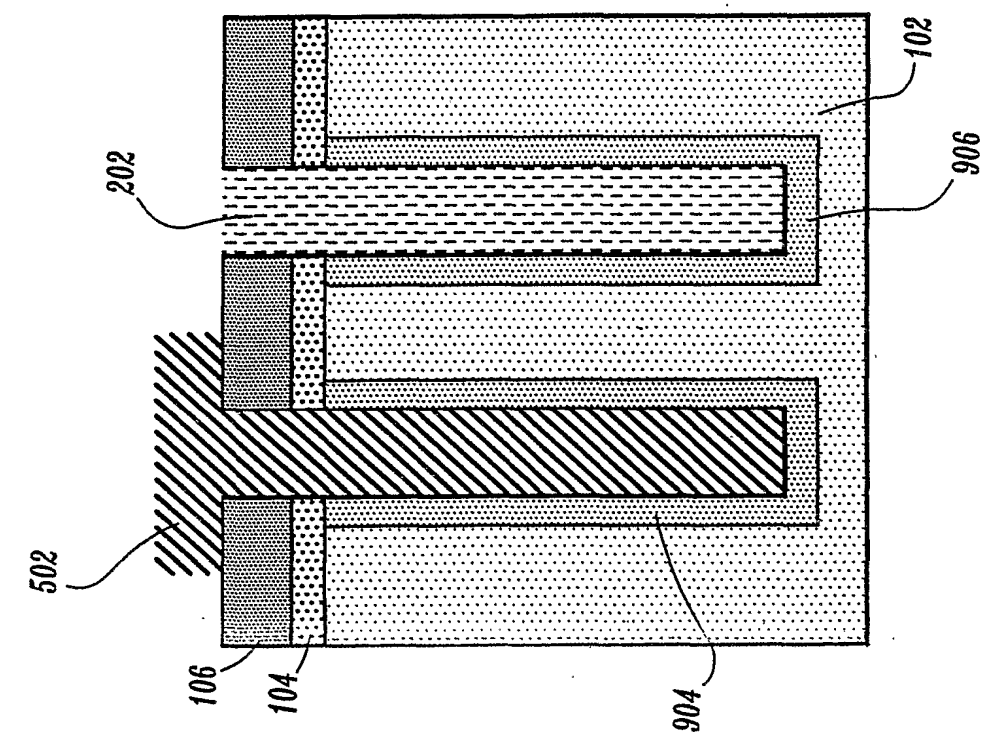

FIG. 12

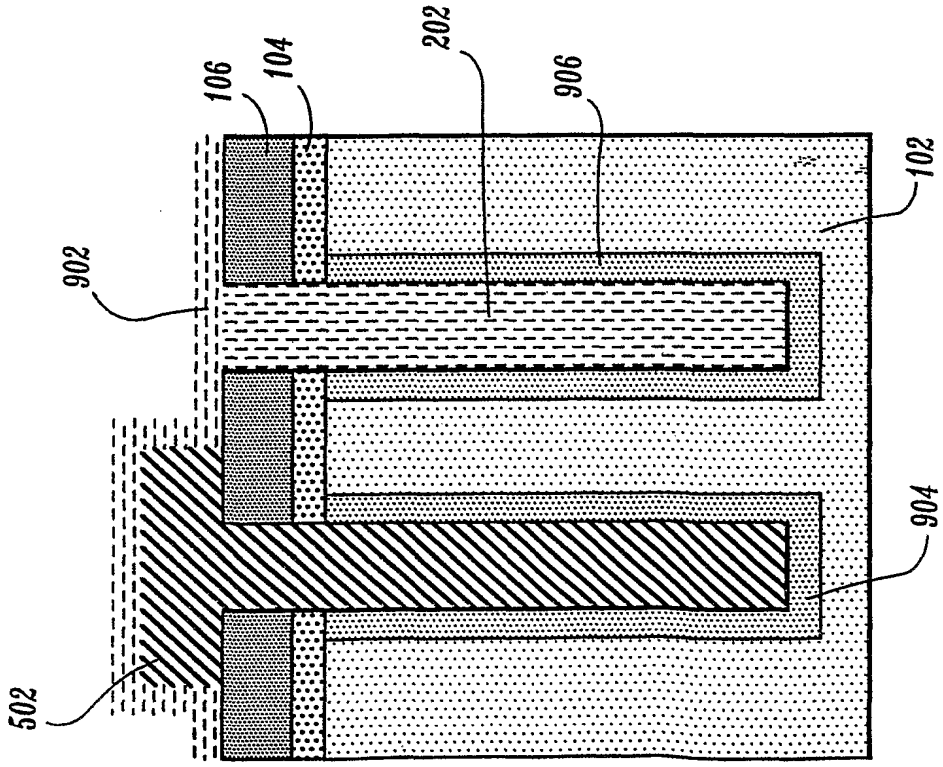

FIG. 11

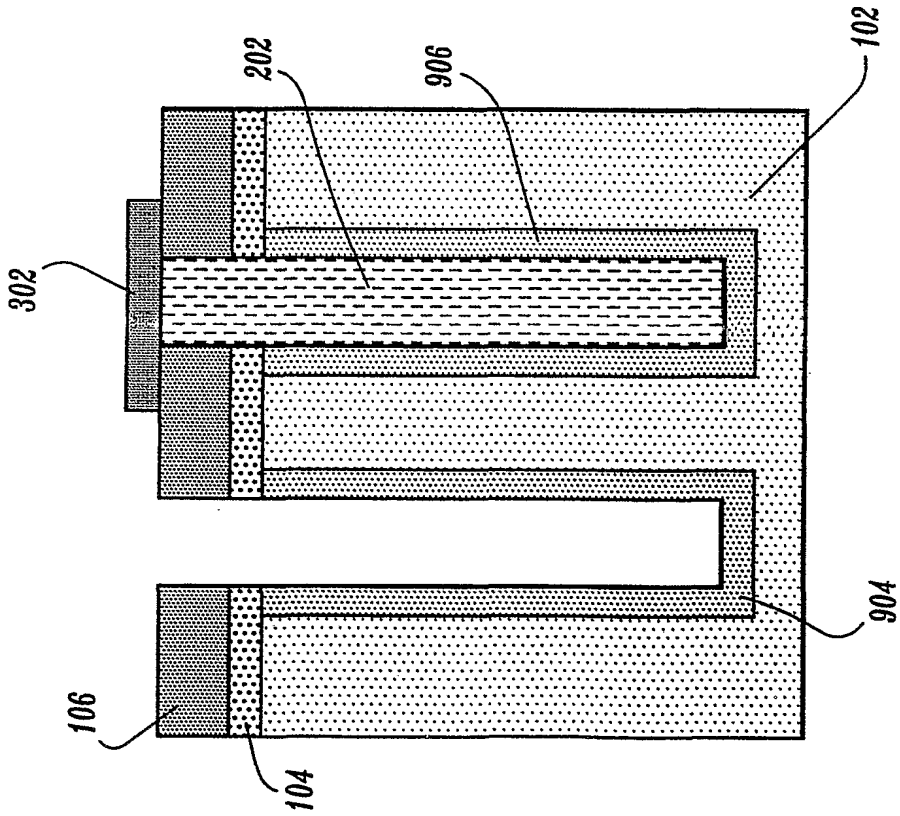

FIG. 13

INTERNATIONAL SEARCH REPORT

International Application No
PCT/GB 02/00659

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L31/103 H01L31/105 H01L27/144 H01L31/0352

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
PAJ, EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 410 175 A (KYOMASU MIKIO ET AL) 25 April 1995 (1995-04-25) figure 9 ---	1-10
A	US 4 112 457 A (D AIELLO ROBERT VINCENT) 5 September 1978 (1978-09-05) abstract; figure 1 ---	
A	HO J Y L ET AL: "HIGH-SPEED AND HIGH-SENSITIVITY SILICON-ON-INSULATOR METAL- SEMICONDUCTOR-METAL PHOTODETECTOR WITH TRENCH STRUCTURE" APPLIED PHYSICS LETTERS, AMERICAN INSTITUTE OF PHYSICS. NEW YORK, US, vol. 69, no. 1, 1 July 1996 (1996-07-01), pages 16-18, XP000599611 ISSN: 0003-6951 figure 1 ---	
	-/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
9 July 2002	17/07/2002

Name and mailing address of the ISA	Authorized officer
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	PATENT ABSTRACTS OF JAPAN vol. 012, no. 342 (E-658), 14 September 1988 (1988-09-14) & JP 63 102282 A (FUJITSU LTD), 7 May 1988 (1988-05-07) abstract	

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International Application No
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